Abstract Of The Disclosure

A graphics system including a custom graphics and audio processor produces exciting 2D and 3D graphics and surround sound. The system includes a graphics and audio processor including a 3D graphics pipeline and an audio digital signal processor. Techniques for efficiently buffering graphics data between a producer and a consumer within a low-cost graphics systems such as a 3D home video game overcome the problem that a small-sized FIFO buffer in the graphics hardware may not adequately load balance a producer and consumer – causing the producer to stall when the consumer renders bit primitives. One aspect of the invention solves this invention by allocating part of main memory to provide a variable number of variable sized graphics commands buffers. Applications can specify the number of buffers and the size of each. All writes to the graphics FIFO can be routed a buffer in main memory. The producer and consumer independently maintain their own read and write pointers, decoupling the producer from the consumer. The consumer does not write to the buffer, but uses its write pointer to keep track of data valid positions within the buffer. The producer can write a read command to a buffer that directs the consumer to read a string of graphics commands (e.g., display list) stored elsewhere in the memory, and to subsequently return to reading the rest of the buffer. Display lists can be created by simply writing a command that redirects the output of the producer to a display list buffer.